AF

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants: Cheisan J. Yue, *et al.*	I hereby certify that this paper is being deposited with the United States Postal Service as first class mail, postage pre-paid, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this date:
Serial No.: 10/040,395	
Filed: January 07, 2002	
For: **VARACTOR WITH IMPROVED TUNING RANGE**	
Group Art Unit: 2811	
Examiner: S. Hu	May 31, 2005 (Date)
Attorney Docket No.: P01,0365	
Confirmation No.: 2072	Trevor B. Joike Reg. No. 25,542 Attorney for Appellants

APPELLANT'S BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the provisions of 37 CFR §1.192, Appellants submit the following brief.

1. Real Party in Interest

The real party in interest is Honeywell International Inc. of Morristown, NJ.

2. Related Appeals and Interferences

There are no other appeals and interferences known to Appellants, Appellants' legal representatives or assignees which will directly affect or be affected by or have a bearing on the Board's decision in the pending appeal.

3. Status of Claims

Claims 32-40 are finally rejected. Claims 1-20 and 30 are withdrawn from consideration.

4. Status of Amendments

All amendments have been entered.

5. Summary of Claimed Subject Matter

As shown in Figures 2 and 3, a varactor 10 is formed on a silicon-on-insulation (SOI) structure 12 having a silicon layer 14 formed over an insulation layer 16. The insulation layer 16, such as SiO_2, is formed over a handle wafer 18. Silicon having a high resistivity may

be used for the handle wafer 18. A plurality of MOS transistors is used to construct the varactor 10.

A cross-sectional side view of one such transistor 20 is shown in Figure 3. The silicon layer 14 of the transistor 20 is doped to form two N+ regions 22 and 24, one of which forms a source and the other of which forms a drain, separated by a P- well 26. A gate oxide 28 is provided over the P- well 26, and a polysilicon gate 30 is provided over the gate oxide 28. The gate oxide 28 and the polysilicon gate 30 are defined by suitable dielectric spacers 32 and 34.

The varactor 10 shown in Figure 2 includes a plurality of transistors each of which may be similar to the transistor 20. Thus, the varactor 10 has a plurality of gates 36. Each of the gates 36 is polysilicon formed over a gate oxide, and each of the gates 36 extends over a corresponding P- well. N+ regions 38 are formed in the silicon layer 14 on each side of each of the gates 36.

A first metal layer 40 is electrically coupled to each of the gates 36, and a second metal layer 42 is electrically coupled to each of the N+ regions 38. The equivalent circuit of the varactor 10 is shown in Figure 6. The varactor 10 has no P+ to P- direct body contact.

Figure 4 is a graph showing the capacitance response of an example construction of the varactor 10. The capacitance of the varactor 10 varies according to the voltage applied across the first and second metal layers 40 and 42. As this voltage increases, the varactor 10 moves from the depletion mode to the inversion mode. During this operation, the potential on the body of the transistor (i.e., the P- wells) is allowed to float with respect to the gates and the source and drain regions. As can be see by the graph of Figure 4, capacitive switching ratio R of the varactor 10 for this example construction is on the order of 33. The capacitive switching ratio R is defined as C_{max}/C_{min}, where C_{max} is the maximum capacitance of the varactor 10, and where C_{min} is the minimum capacitance of the varactor 10.

Figure 5 is a graph showing the capacitance response of another example construction of the varactor 10. As can be seen by the graph of Figure 5, the capacitive switching ratio R of the varactor 10 in this case is on the order of 5.

6. Grounds of Rejection to be Reviewed on Appeal

1) Whether claims 32-40 are unpatentable under 35 U.S.C. §103(a) over U.S. Patent No. 5,038,184

(hereinafter, "the Chiang '184 patent") in view of U.S. Patent No. 6,100,770 (hereinafter, "the Litwin '770 patent").

2) Whether the objection to independent claim 32 is properly founded.

For purposes of this appeal, dependent claims 33, 36, and 38 may be grouped with independent claim 32.

7. Argument

The Chiang '184 Patent

In Figure 1, the Chiang '184 patent discloses a varactor 31 having an active semiconductor layer 32 sandwiched between a dielectric 33 and an n-type ground electrode 34. A gate electrode 35 is deposited on top of the dielectric film 33. (It is noted that, based upon the text of the Chiang '184 patent, the reference numeral 33 should point to the layer denoted by t_d and the reference numeral 32 should point to the layer denoted by t_{si}.) The varactor 31 includes an insulating substrate 36, and the ground electrode 34 sits on the insulating substrate 36.

The varactor 31 is switched back and forth between its maximum capacitance accumulation mode and its minimum capacitance depletion mode by reversing the

polarity of its gate voltage V_G. Accordingly, whenever the gate 35 of the varactor 31 is positively biased, electrons are accumulated in the silicon layer 32 near its interface with the dielectric film 33. Conversely, when the gate 35 is sufficiently negatively biased, the silicon layer 32 is depleted of electrons.

The Chiang '184 patent states that, if the active silicon layer 32 is single crystal silicon, capacitive switching ratios R well in excess of two can be achieved. However, according to the Chiang '184 patent, existing single crystal silicon technology is not applicable to the fabrication of large area integrated circuits, and it is difficult to obtain high capacitive switching ratios R for the varactor 31 if its active semiconductor layer 32 is composed of amorphous silicon.

The Chiang '184 patent, therefore, also discloses a varactor 41 in Figures 2 and 3. The varactor 41 has smaller effective capacitive surface areas in depletion than in accumulation, and the varactor 41 uses poly-silicon thin films. The varactor 41 has a ground layer 42 of un-doped or very lightly doped silicon on a thick insulating substrate 43. A thin dielectric film 44 is formed on the ground layer 42, and a metal or silicon

p+ or n+ gate electrode 46 is deposited on the dielectric film 44.

N+ or p+ ground electrodes 45 are formed in the ground layer 42 so that they only partially and laterally overlap the gate electrode 46. As a result, the gate electrode 46 longitudinally aligns with a section 47 of the active silicon layer 42 which is between the ground electrodes 45 and which is in intimate electrical contact with the substrate 43.

The Chiang '184 patent states that the capacitive switching ratio R for the varactor 41 is controlled by the ground-gate overlap. In other words, the capacitive switching ratio R for the varactor 41 is equal to the ratio of the length L of the gate to the ground overlap length $2L_2$. The Chiang '184 patent further states that there is a performance tradeoff between switching speed and RF impedance on the one hand and capacitive switching ratio R on the other. Thus, switching speed can be increased and RF impedance can be lowered at the cost of decreased capacitive switching ratio R. Alternatively, the capacitive switching ratio R can be increased at the cost of decreased switching speed and increased RF impedance.

A varactor 51 as shown in Figure 4 is a bottom-gate counterpart to the varactor 41.

Figures 5 and 6 show top-gate and bottom-gate varactors 61 and 62, respectively. The ground electrodes 45 of the varactors 61 and 62 reside in a suitably patterned conductive layer 63 which is physically distinct from the active silicon film 42, but which is in intimate contact therewith in partially overlapping alignment with the gate electrode 46. Again, the capacitive switching ratios R for the varactors 61 and 62 are controlled by their respective ground-gate overlaps.

A top-gate varactor 71 shown in Figures 7 and 8 has gate electrode segments 46a-46m and ground electrode segments 45a-45n which are laterally staggered with respect to the gate electrode segments 46a-46n, where n = m + 1. Each of the gate electrode segments 46a-46m is partially and laterally overlapped by two of the ground electrode segments 45a-45n such that neighboring gate electrode segments share the ground electrode segments that are disposed between them. The gate electrode segments 46a-46m are electrically interconnected, and the ground electrode segments 45a-45n are electrically interconnected.

Figure 9 illustrates a varactor 81 which is a bottom-gate counterpart to the varactor 71.

The Litwin '770 Patent

The Litwin '770 patent discloses in Figure 2 a varactor 20 comprising an NMOS enhancement transistor. The transistor is formed in a p silicon substrate 21. A p well 22 is formed in the p silicon substrate 21, and an n+ source 23 and an n+ drain 24 are formed in the p well 22. The impurity concentration of the source and drain regions 23 and 24 is greater than the impurity concentration of the p well 22. An insulating layer 25, preferably of silicon oxide, is formed on the substrate 21, and a poly-silicon gate 26 is formed on the insulating layer 25 such that the gate 26 is electrically insulated from the p well 22. A common electrode C_A of the varactor 20 is formed by connecting the source 23 to the drain 24. A second electrode C_B of the varactor 20 is connected to the gate 26.

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Independent claim 32 is directed to a method of making a varactor. A plurality of alternating P- wells and N+ regions are formed in a silicon layer of an SOI

structure. The P- wells form N+/P- junctions with the N+ regions, and each of the P- wells and the N+ regions extends completely through the silicon layer to an insulation layer of the SOI structure. A plurality of gate oxides are formed such that each of the gate oxides is formed above a corresponding one of the P- wells. A plurality of silicon gates are formed such that each of the silicon gates is formed above a corresponding one of the gate oxides. The silicon gates are electrically coupled together, and the N+ regions are electrically coupled together.

The Examiner recognizes that the Chiang '184 patent does not disclose a varactor having a plurality of alternating P- type wells and N+ type regions in a silicon layer. Therefore, the Examiner relies on Figure 2 of the Litwin '770 patent which shows a varactor 20 having n+ type source and drain regions and a p type well. The Examiner then argues that, because lightly doped well regions are desirable as evidenced by the Litwin '770 patent, it would have been obvious to incorporate such lightly doped well regions in the varactors disclosed in the Chiang '184 patent to form varactors having a plurality of alternating P- type wells and N+ type regions in a silicon layer.

However, there are a number of problems with this argument.

First, the Examiner argues that the particular combination of the Chiang '184 patent and the Litwin '770 patent as espoused by the Examiner is desirable, but the Examiner does not explain what would make this combination desirable to one of ordinary skill in the art. The argument that this combination is desirable is merely a conclusion. The Examiner has failed to explain why such a combination is desirable or what would have motivated one skilled in the art to combine the teachings of the Chiang '184 patent and of the Litwin '770 patent. Therefore, the Examiner has not made out a prima facie case of obviousness.

Accordingly, for this first reason, independent claim 32 is not obvious over the Chiang '184 patent in view of the Litwin '770 patent.

Second, the Litwin '770 patent in Figure 2 discloses n+ source and drain regions 23 and 24 formed in a p well 22. The nomenclature (p instead of p+ or p-) as used in Figure 2 indicates that the well 22 is moderately doped (p) instead of lightly doped (p-).

Therefore, the Litwin '770 patent does not suggest a varactor with alternating p- wells and n+ regions.

The Chiang '184 patent discloses that the silicon 42 can be undoped or lightly doped. However, the Chiang '184 patent does not disclose or suggest whether, if the silicon film 42 is to be lightly doped, the silicon 42 should be lightly doped with p-type impurities to produce p- regions. Moreover, the Chiang '184 patent does not disclose or suggest whether, if the silicon film 42 is to be lightly doped, the silicon 42 should be doped so as produce alternating lightly doped p- regions and heavily doped n+ regions.

Accordingly, neither the Litwin '770 patent nor the Chiang '184 patent discloses or suggests forming a varactor by lightly doping the silicon 42 with p-type impurities to produce p- regions and heavily doping the silicon 42 with n-type impurities to produce n+ regions.

Therefore, for this second reason, independent claim 32 is not obvious over the Chiang '184 patent in view of the Litwin '770 patent.

Third, the Chiang '184 patent discloses in column 1, lines 5-18 that its varactor is intended for integrated circuits. Also, the dashed lines in Figure 2

of the Chiang '184 patent seem to suggest that the electrode 45 are doped down to the dielectric layer 43 such that the electrodes 45 are not formed in a well region.

The Litwin '770 patent, on the other hand, discloses in column 7, lines 18-32 that the source and drain regions 23 and 24 need to be formed in the well region 22 when the varactor is to be integrated with other devices (thereby producing an integrated circuit).

Therefore, because of these conflicting disclosures, the Litwin '770 patent suggests that it cannot be combined with the Chiang '184 patent so as to meet the limitations of independent claim 32.

Accordingly, for this third reason, independent claim 32 is not obvious over the Chiang '184 patent in view of the Litwin '770 patent.

Fourth, the Chiang '184 patent discloses that the capacitive switching ratio R of its varactor is dependent on the gate-ground overlap ratio. Thus, the Chiang '184 patent discloses that the capacitive switching ratio R can be increased by increasing gate length versus ground overlap length.

On the other hand, the Litwin '770 patent discloses that the capacitive switching ratio R (referred

to in the Litwin '770 patent as dynamic range) of its varactor can be made high by making the well as lightly doped as possible at its principal surface region (i.e., under the gate 36 and near the insulating layer 25). Indeed, the Litwin '770 patent discloses that additional doping of the well should be blocked. Thus, the well region 22 starts out as a moderately doped region, as indicated by the p notation in Figure 2. The Litwin '770 patent then discloses that the well region 22 should receive little additional doping.

Accordingly, the Chiang '184 patent and the Litwin '770 patent suggests solutions to increasing the capacitive switching ratio R that are not compatible. That is, the Litwin '770 patent suggests controlling doping so that the portion of the well 32 between the source and drain regions 23 and 24 receive no dopant, whereas the Chiang '184 patent discloses doping such that the dopant migrates through the well toward the opposite source or drain region.

Consequently, one of ordinary skill in the art would not combine the Chiang '184 patent and the Litwin '770 patent as suggested by the Examiner so as to meet the limitations of independent claim 32.

Therefore, for this fourth reason, independent claim 32 is not obvious over the Chiang '184 patent in view of the Litwin '770 patent.

Because independent claim 32 is patentable over the Chiang '184 patent in view of the Litwin '770 patent, dependent claims 33-40 are similarly patentable over the Chiang '184 patent in view of the Litwin '770 patent.

Moreover, dependent claim 34 requires the SOI structure recited in independent claim 32 to include a layer of high resistivity silicon under the insulation layer.

The Litwin '770 patent does not disclose an SOI structure, and the Chiang '184 patent does not disclose that the insulating layer 43 is over a silicon layer or that such a silicon layer is high resistivity silicon. Accordingly, the combination of the Chiang '184 patent and the Litwin '770 patent does not disclose or suggest the invention of dependent claim 34.

Furthermore, the Examiner contends that it is well known that silicon handle layers below the insulating layers of SOI structures are highly resistive. However, the Examiner has not shown that it would have been obvious to provide the Chiang/Litwin varactor in an SOI structure having a highly resistive silicon

substrate. The Examiner has only argued that SOI structures with highly resistive silicon substrate are known.

Accordingly, the Examiner has not made out a prima facie case of obviousness with respect to dependent claim 34.

Therefore, dependent claim 34 is not obvious over the Chiang '184 patent in view of the Litwin '770 patent.

Dependent claim 35 recites that the insulation layer comprises sapphire.

Neither the Chiang '184 patent nor the Litwin '770 patent discloses a sapphire insulation layer. Accordingly, the combination of the Chiang '184 patent and the Litwin '770 patent does not disclose or suggest the invention of dependent claim 35.

Moreover, the Examiner does not specifically address the use of sapphire in the Final Rejection. Accordingly, the Examiner has not made out a prima facie case of obviousness with respect to dependent claim 34.

Therefore, dependent claim 35 is not obvious over the Chiang '184 patent in view of the Litwin '770 patent.

Dependent claim 37 recites that the P- wells form a transistor body, and that the transistor body is allowed to float.

Neither the Chiang '184 patent nor the Litwin '770 patent discloses or suggests this feature. Accordingly, the combination of the Chiang '184 patent and the Litwin '770 patent does not disclose or suggest the invention of dependent claim 37.

The Examiner contends that the p type body (presumably the well 22 disclosed in the Litwin '770 patent) would form a p/n junction which, according to the Examiner, would naturally be allowed to float. However, the Examiner's contention is a mere conclusion not supported by evidence. Moreover, the Examiner is presumably referring to transistors and has not established a nexus between transistors and varactors with respect to floating bodies.

Therefore, dependent claim 37 is not obvious over the Chiang '184 patent in view of the Litwin '770 patent.

Dependent claims 39 and 40 recite that the capacitive switching ratio is equal to or greater than 5 and 20, respectively. The only capacitive switching ratio mentioned in the Chiang '184 patent is greater than

2, and the Litwin '770 patent does not mention any specific capacitive switching ratios.

The Examiner argues that a high capacitive switching ratio is desirable. However, neither the Chiang '184 patent nor the Litwin '770 patent disclose how to achieve a capacitive switching ratio equal to or greater than 5.

The Examiner also argues that the gate width to gate length ratios given in the Litwin '770 patent at column 6, lines 10-17 are similar to those given in the present application. The Examiner, however, has not demonstrated (i) what specific gate and width lengths from the Litwin '770 patent produce the same gate width to gate length ratios as disclosed in the present application, (ii) why these gate width to gate length ratios are even pertinent to capacitance switching ratios, and (iii) that the number of gates disclosed in either the Chiang '184 patent or the Litwin '770 patent will produce the claimed capacitance switching ratios.

Therefore, dependent claims 39 and 40 are not obvious over the Chiang '184 patent in view of the Litwin '770 patent.

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The Examiner has objected to claim 40 as not being supported by the original disclosure, and specifically objected to Figure 4 and the disclosure for failing to disclose a capacitive switching ratio equal to or greater than 20.

However, as disclosed in the original specification, Figure 4 shows a capacitive switching ratio for the varactor 10 that is on the order of 33. Thus, as shown in Figure 4, C_{max} is on the order of 33 pf and C_{min} is on the order of 1 pf. As can be seen, the Examiner misinterpreted Figure 4 and the specification. Accordingly, claim 40 is consistent with the specification and the drawings.

8. Appendix

The Appendix containing a copy of the appealed claims is attached hereto.

9. Evidence Appendix

There is no evidence submitted under §§ 1.130, 1,131, or 1.132.

10. Related Proceedings Appendix

There are no other appeals and interferences known to Appellants, Appellants' legal representatives or assignees which will directly affect or be affected by or have a bearing on the Board's decision in the pending appeal.

11. Conclusion

For the foregoing reasons, reversal of the Final Rejection is respectfully requested.

This brief is being filed in triplicate as required by 37 C.F.R. §1.192.

The fee set forth in 37 C.F.R. §1.17(c) is enclosed herein by check. The Commissioner is hereby authorized to charge any deficiency in the amount enclosed or any additional fee which may be required to Deposit Account No. 50-1519.

Respectfully submitted,

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May 31, 2005

APPENDIX

32. A method of making a varactor comprising:

forming a plurality of alternating P- wells and N+ regions in a silicon layer of an SOI structure, wherein the P- wells form N+/P- junctions with the N+ regions, and wherein each of the P- wells and the N+ regions extends completely through the silicon layer to an insulation layer of the SOI structure;

forming a plurality of gate oxides, wherein each of the gate oxides is formed above a corresponding one of the P- wells;

forming a plurality of silicon gates, wherein each of the silicon gates is formed above a corresponding one of the gate oxides;

electrically coupling each of the silicon gates together; and,

electrically coupling each of the N+ regions together.

33. The method of claim 32 wherein each of the silicon gates comprises a polysilicon gate.

34. The method of claim 32 wherein the SOI structure includes a layer of high resistivity silicon under the insulation layer over.

35. The method of claim 32 where in the insulation layer comprises sapphire.

36. The method of claim 32 where in the insulation layer comprises an oxide.

37. The method of claim 32 wherein the P-wells form a transistor body, and wherein the transistor body is allowed to float.

38. The method of claim 32 wherein each of the silicon gates is formed so as to have a width to length ratio of approximately 16 to 1.

39. The method of claim 32 wherein the varactor has a capacitive switching ratio equal to or greater than 5.

40. The method of claim 32 wherein the varactor has a capacitive switching ratio equal to or greater than 20.